In the Claims:

Please amend the claims as indicated below. The amendments are supported by the application as originally filed and no new matter has been added. For instance, the amendment to claim 1, which is intended to clarify the claim, is supported by Fig. 6 and accompanying text. Claim 10 was amended to correct dependency and a typographical error. Added text has been underlined, deleted text has been struck through. Please cancel claims 5-7.

1. (currently amended) A method of synchronous reading for a plurality of words in a memory system, comprising:

selecting said plurality of words to be read, ~~each of~~ said selected plurality of words having a first group of words and at least one subsequent group of words;

reading said first group of words of said selected plurality of words into a plurality of data registers during a latency period; and

shifting out each word of said first group of words of said selected plurality of words synchronously at the end of said latency period, one word of the first group of words shifted out at each clock cycle following the latency period until each word of the first group of words has been shifted out.

2. (previously presented) The method of claim 1, wherein said step of reading further comprises the following steps:

determining from said selected plurality of words which said first group of words is to be read, said first group of words having a first tier and a subsequent tier;

reading said first tier of said first group of words into said plurality of data registers at the beginning of said latency period;

deleting said first tier of said first group of words from said plurality of data registers after said reading step during said latency period;

loading said first tier of said subsequent group of words into said plurality of data registers after said step of deleting during said latency period; and

reading said subsequent tier of said first group of words into said plurality of data registers after said step of loading during said latency period.

3. (original) The method of claim 2, wherein the step of determining which said first group of words to be read further comprising:

checking whether an address field of said first group of words to be read belongs to a first address field or a subsequent address field, if said address field of said first group of words belongs to said first address field then

selecting said first tier of words whose address coincides with an initial address of said first tier of words; otherwise

selecting said first group of words whose address coincides with an initial address of subsequent tier of words.

4. (original) The method of claim 2, wherein the step of reading said first tier of said first group of words further comprises checking whether a last bit of said first tier of words has been reached, if said last bit of said first tier of words has not been reached, continuing reading; otherwise continuing to read said subsequent tier of words.

5. (cancelled)

6. (cancelled)

7. (cancelled)

8. (currently amended) A two-tier column decoder to facilitate synchronous reading of a plurality of words in a memory system, comprising:

a most-significant-bit decoding means for decoding a most significant bit of said plurality of words to be read and determining whether an address of said plurality of words is a lower or a higher address, said means being coupled to a main bit line of said memory system;

a first selecting means for selecting for selecting both even and odd addresses for a first reading during a latency period, said first selecting means coupled to said ~~first~~ decoding means; ~~and~~

a second selecting means coupled to said ~~second~~ first selecting means, said second selecting means for selecting either an even or address for a subsequent reading;

wherein the first and second selecting means each have a plurality of input terminals, an output terminal, and a feedback terminal for determining whether said plurality of words is either said odd or even address.

9. (cancelled)

10. (currently amended) The two-tier column decoder of claim ~~8~~ 9, wherein each ~~decoding~~ selecting means further comprises:

a first logic means adapted to receive said plurality of input terminals for producing a status signal of said plurality of input signals;

a second logic means adapted to receive said status signals for producing a signal that determines whether said plurality of input terminals are in said even or odd address;

a plurality of transistor feedback means adapted to receive a feedback output signal from a subsequent decoding means and coupled to said logic means for providing a status of said subsequent decoding means.

11. (currently amended) A burst mode operation system for fast synchronous reading of a memory system, comprising:

a burst controller adapted to receive an input clock signal, a variable latency signal, and a burst sequence control signal from said memory system to produce a plurality of words to be read and an output clock signal, the burst controller further comprising:

a clock driver adapted to receive said input clock signal to produce an internal and an external clock signal;

a burst control and ready generator adapted to receive said internal clock signal, said external clock signal for producing said output clock signal and a page boundary signal;

a word counter coupled to said output clock signal for producing a plurality of word address counts;

a burst sequence control adapted to receive one of said plurality of word address counts and said output clock signal for producing a plurality of read signals; and

a word generator coupled to said word counter and a word output controller for producing said plurality of words to be read;

an address controller coupled to said burst controller for producing addresses of said plurality of words to be read;

a two-tier column decoder adapted to receive said addresses from said address controller for producing a first tier address and a second tier address; and

a row decoder adapted to receive said addresses from said address controller for producing row addresses of said plurality of words to be read.

12. (cancelled)

13. (original) The burst mode operation system of claim 11, wherein said address controller further comprises:

a burst control clock device adapted to receive said output clock signal, said plurality of word address counts to produce at least one burst control clock signal;

a Y-address register and counter adapted to receive said output clock signal and said addresses of said plurality of words;

an end of page detector adapted to receive a plurality of address counter signals from said Y-address register and counter to produce an end of page signal;

an X-address clock adapted to receive said end of page signal to produce an X-clock signal; and

an X-address register and counter adapted to receive said X-clock signal, and addresses of said plurality of words to be read.

14. (previously presented) A two-tier column decoder to facilitate synchronous reading of a plurality of words in a memory system, comprising:

a sub bitline decoder coupled to a main bit line of said memory system for decoding a most significant bit of said plurality of words to be read and for determining whether an address of said plurality of words is for a lower or higher word address;

a first tier decoder coupled to said sub bitline decoder to select both said even and odd addresses of said plurality of words for a first reading during a latency period; and

a second tier decoder coupled to said first tier decoder to select either said lower or higher word addresses for a subsequent reading, said second tier decoder including an array of decoder blocks coupled to one another, each having a plurality of input terminals, an output terminal, and a feedback terminal for determining whether addresses of said plurality of words is said lower or higher order.

15. (previously presented) The two-tier column decoder system of claim 14, wherein each decoder block further comprises:

a first NOR logic gate adapted to receive said plurality of input terminals;

a second NOR logic gate adapted to receive an output of said first NOR logic gate; and

a plurality of transistors coupled together to receive a feedback signal from a subsequent decoder block and coupled to said second NOR logic gate.